

01-10-00 A

Case Docket No. 98RO21654163

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Transmitted herewith for filing is the patent application of:

Inventors: Franck ROCHE

For: MICROPROCESSOR WITH PROTECTION CIRCUITS TO SECURE THE ACCESS TO
ITS REGISTERS

Enclosed are:

- (X) Patent Application: 14 pages, 9 claims.
- (X) 3 Sheets of drawings.
- (X) Citation Under 37 CFR 1.97 and PTO-1449.
- (X) Preliminary Amendment.
- (X) Submission of Proposed Drawing Modification.

The Declaration and Filing Fee are NOT ENCLOSED.

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For: MICROPROCESSOR WITH PROTECTION)
CIRCUITS TO SECURE THE ACCESS TO)
ITS REGISTERS)

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PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to the calculation of fees and examination of
the present application, please enter the amendments and
remarks set out below.

In the Drawings:

Submitted herewith is a request for proposed drawing
modifications as indicated in red ink to label the blocks in
FIGS. 1-4.

In the Claims:

Please cancel Claims 1-9.

Please add new Claims 10-42.

10. A microprocessor comprising:
an address bus;
a data bus;
a plurality of read and write accessible registers
connected to said data bus;

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an address decoder connected to said address bus for selecting said plurality of registers as a function of an address provided by said address bus; and

a plurality of protection circuits connected between said address decoder and said plurality of registers, each protection circuit associated with a register to secure access thereto by blocking selection of said register after each resetting of the microprocessor, and releasing of said protection circuit by a successive sending on said data bus of N passwords proper to said register during N first operations for selection of said register with $N \geq 1$, the selection of said associated register being effective only for subsequent operations for the selection thereof until a next resetting of the microprocessor.

11. A microprocessor according to Claim 10, wherein each protection circuit is arranged to block the selection of said associated register during read and write access operations to said associated register after each resetting of the microprocessor.

12. A microprocessor according to Claim 10, wherein each protection circuit is arranged to block the selection of said associated register during write access operations to said associated register after each resetting of the microprocessor.

13. A microprocessor according to Claim 10, wherein each protection circuit is connected between an output of said address decoder and a selection input of said associated register for selection thereof.

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14. A microprocessor according to Claim 10, wherein each protection circuit, during the N first operations for the selection of said associated register, compares N data elements present on said data bus with the N passwords proper to said associated register, and each protection circuit is released for subsequent operations of selection of said associated register until the next resetting of the microprocessor if the N data elements correspond to the N passwords.

15. A microprocessor according to Claim 10, wherein a single password is provided for each register; and wherein each protection circuit comprises:

a comparator circuit for comparing, during a first operation for the selection of said register, a data element present on said data bus with the password proper to said register and for delivery of an output signal representing a result of the comparison;

first means for holding in each protection circuit the output signal until the next resetting of the microprocessor; and

second means permitting the selection of said register if the output signal indicates that the data present on said data bus during the first operation of selection of said register corresponds to the password associated with said register.

16. A microprocessor according to Claim 15, wherein said first means comprises first and second D type flip-flop circuits, each flip-flop circuit having a clock input, a signal input, a resetting input to which a signal for resetting the microprocessor is applied, and an output;

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said first flip-flop circuit having the clock input connected to the output of said address decoder responsible for selecting said register associated with said protection circuit, and the signal input for receiving a signal corresponding to a logic signal; and

said second flip-flop circuit having the clock input connected to the output of said first flip-flop circuit, the signal input for receiving the output signal of said comparator circuit, and an output which delivers the output signal of said comparator circuit until the next resetting of the microprocessor.

17. A microprocessor according to Claim 16, wherein said second means comprises:

a delay circuit;

a two-input AND logic gate having a first input connected to the output of said address decoder for selecting the register associated with said protection circuit, a second input connected through said delay circuit to the output of said second flip-flop circuit of said first means, and an output connected to the selection input of said associated register.

18. A microprocessor according to Claim 17, wherein said delay circuit comprises a shift register synchronized with the operations for the selection of said associated register.

19. A microprocessor comprising:

an address bus;

a data bus;

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a plurality of read and write accessible registers connected to said data bus;

an address decoder connected to said address bus for selecting said plurality of registers as a function of an address provided by said address bus; and

a plurality of protection circuits connected between said address decoder and said plurality of registers, each protection circuit associated with a register to secure access thereto by blocking selection of said register during write access operations after each resetting of the microprocessor, and releasing of said protection circuit by a successive sending on said data bus of N passwords proper to said register during N first operations for selection of said register with $N \geq 1$, the selection of said associated register being effective only for subsequent operations for the selection thereof until a next resetting of the microprocessor.

20. A microprocessor according to Claim 19, wherein each protection circuit is connected between an output of said address decoder and a selection input of said associated register for selection thereof.

21. A microprocessor according to Claim 19, wherein each protection circuit, during the N first operations for the selection of said associated register, compares N data elements present on said data bus with the N passwords proper to said associated register, and each protection circuit is released for subsequent operations of selection of said associated register until the next resetting of the microprocessor if the N data elements correspond to the N passwords.

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22. A microprocessor according to Claim 19, wherein a single password is provided for each register; and wherein each protection circuit comprises:

a comparator circuit for comparing, during a first operation for the selection of said register, a data element present on said data bus with the password proper to said register and for delivery of an output signal representing a result of the comparison;

first means for holding in each protection circuit the output signal until the next resetting of the microprocessor; and

second means permitting the selection of said register for the subsequent selection operations of said register if the output signal indicates that the data present on said data bus during the first operation of selection of the register corresponds to the password associated with said register.

23. A microprocessor according to Claim 22, wherein said first means comprises first and second D type flip-flop circuits, each flip-flop circuit having a clock input, a signal input, a resetting input to which a signal for resetting the microprocessor is applied, and an output;

said first flip-flop circuit having the clock input connected to the output of the address decoder responsible for selecting said register associated with said protection circuit, and the signal input for receiving a signal corresponding to a logic signal; and

said second flip-flop circuit having the clock input connected to the output of said first flip-flop circuit, the signal input for receiving the output signal of said

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comparator circuit, and an output which delivers the output signal of said comparator circuit until the next resetting of the microprocessor.

24. A microprocessor according to Claim 23, wherein said second means comprises:

a delay circuit;

a first two-input AND logic gate having a first input connected to the output of said address decoder which has the task of selecting the register associated with said protection circuit, and a second input connected through said delay circuit to the output of said second flip-flop circuit of said first means;

a second two-input AND logic gate having a first input connected to the output of said address decoder which has the task of selecting the register associated with said protection circuit, and a second input receiving a read/write signal; and

an OR logic gate having a first input connected to an output of said first two-input AND logic gate, and a second input connected to an output of said second two-input AND logic gate, and an output connected to said register.

25. A microprocessor according to Claim 24, wherein said delay circuit comprises a shift register synchronized with the operations for the selection of said associated register.

26. A microprocessor comprising:
an address bus;
a data bus;

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a plurality of read and write accessible registers connected to said data bus;

an address decoder connected to said address bus for selecting said plurality of registers as a function of an address provided by said address bus; and

a plurality of protection circuits connected between said address decoder and said plurality of registers;

each protection circuit associated with a register to secure access thereto by blocking selection of said register after each resetting of the microprocessor, at least two passwords are provided to each register, and releasing of said protection circuit by a successive sending on said data bus of at least $2N$ passwords proper to said register during N first operations for selection of said register with $N \geq 1$, the selection of said associated register being effective only for subsequent operations for the selection thereof until a next resetting of the microprocessor.

27. A microprocessor according to Claim 26, wherein the at least two passwords for said associated register are provided over said data bus in a predetermined order.

28. A microprocessor according to Claim 26, wherein each protection circuit is arranged to block the selection of said associated register during read and write access operations to said associated register after each resetting of the microprocessor.

29. A microprocessor according to Claim 26, wherein each protection circuit is arranged to block the selection of said associated register during write access operations to

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said associated register after each resetting of the microprocessor.

30. A microprocessor according to Claim 26, wherein each protection circuit is connected between an output of said address decoder and a selection input of said associated register for selection thereof.

31. A microprocessor according to Claim 26, wherein each protection circuit, during the N first operations for the selection of said associated register, compare at least $2N$ data elements present on said data bus with the at least $2N$ passwords proper to said associated register, and each protection circuit is released for subsequent operations of selection of said associated register up to the next resetting of the microprocessor if the at least $2N$ data elements correspond to the at least $2N$ passwords.

32. A microprocessor according to Claim 26, wherein each protection circuit comprises:

a first protection circuit portion comprising
 a first comparator circuit for comparing,
 during a first operation for the selection of said register, a data element present on said data bus with a first one the at least two passwords proper to said register and for delivery of an output signal representing a result of the comparison, and
 first means for holding in each protection circuit the output signal until the next resetting of the microprocessor; and
 a second protection circuit portion connected to an output of said first protection circuit portion and comprising

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a second comparator circuit for comparing, during the first operation for the selection of said register, the data element present on said data bus with a second one of the at least two passwords proper to said register and for delivery of an output signal representing a result of the comparison,

second means for holding in each protection circuit the output signal until the next resetting of the microprocessor, and

third means permitting the selection of said register for the subsequent selection operations of said register if the output signal indicates that the data present on said data bus during the first operation of selection thereof corresponds to the at least two passwords associated with said register.

33. A microprocessor according to Claim 32, wherein said first means comprises first and second D type flip-flop circuits, each flip-flop circuit having a clock input, a signal input, a resetting input to which a signal for resetting the microprocessor is applied, and an output;

said first flip-flop circuit having the clock input connected to the output of the address decoder responsible for selecting said register associated with said protection circuit, and the signal input for receiving a signal corresponding to a logic signal;

said second flip-flop circuit having the clock input connected to the output of said first flip-flop circuit, the signal input for receiving the output signal of said comparator circuit, and an signal output which delivers the

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output signal of said comparator circuit until the next resetting of the microprocessor; and

a first delay circuit connected to the output of said second flip-flop circuit.

34. A microprocessor according to Claim 33, wherein said second means comprises third and fourth D type flip-flop circuits, each flip-flop circuit having a clock input, a signal input, a resetting input to which a signal for resetting the microprocessor is applied, and an output;

said third flip-flop circuit having the clock input connected to the output of said first delay circuit for selecting said register associated with said protection circuit, and the signal input for receiving a signal corresponding to a logic signal; and

said fourth flip-flop circuit having the clock input connected to the signal output of said third flip-flop circuit, the signal input for receiving the output signal of said comparator circuit, and an output which delivers the output signal of said comparator circuit until the next resetting of the microprocessor.

35. A microprocessor according to Claim 34, wherein said third means comprises:

a second delay circuit; and

a two-input AND logic gate having a first input connected to the output of said address decoder which has the task of selecting the register associated with said protection circuit, a second input connected through said second delay circuit to the output of said fourth flip-flop circuit of said first means, and an output connected to the selection input of said associated register.

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36. A microprocessor according to Claim 35, wherein said first and second delay circuits each comprises a shift register synchronized with the operations for the selection of said associated register.

37. A method for securing access to a plurality of registers of a microprocessor, the method comprising the steps of:

selecting one of said plurality of registers via an address decoder as a function of an address provided by an address bus connected to the address decoder;

blocking selection of the plurality of registers via a plurality of protection circuits after each resetting of the microprocessor; and

releasing a protection circuit associated with a selected register by successive sending on the data bus N passwords proper to the selected register during N first operations for selection of the register with $N \geq 1$, the selection of the register being effective only for subsequent operations for the selection thereof until a next resetting of the microprocessor.

38. A method according to Claim 37, wherein the step of blocking comprises blocking selection of a selected register during read and write access operations to that register after each resetting of the microprocessor.

39. A method according to Claim 37, wherein the step of blocking comprises blocking selection of a selected register during write access operations to that register after each resetting of the microprocessor.

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40. A method according to Claim 37, wherein each protection circuit is connected between an output of the address decoder and a selection input of an associated register for selection thereof.

41. A method according to Claim 37, wherein each protection circuit, during the N first operations for the selection of an associated register, compares N data elements present on the data bus with the N passwords proper to the associated register, and each protection circuit is released for subsequent operations of selection of the associated register until the next resetting of the microprocessor if the N data elements correspond to the N passwords.

42. A method according to Claim 37, wherein a single password is provided for each register; and wherein the steps of blocking and releasing comprises:

comparing, during a first operation for the selection of the register, a data element present on the data bus with the password proper to the register and for delivery of an output signal representing a result of the comparison;

holding in each protection circuit the output signal until the next resetting of the microprocessor; and

permitting the selection of the register for the subsequent selection operations of the register if the output signal indicates that the data present on the data bus during the first operation of selection of the register corresponds to the password associated with the register.

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REMARKS

It is believed that all of the claims are patentable over the prior art. Accordingly, after the Examiner completes a thorough examination and finds the claims patentable, a Notice of Allowance is respectfully requested in due course. Should the Examiner determine any minor informalities that need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number below.

Respectfully submitted,

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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"EXPRESS MAIL" MAILING LABEL NUMBER EL436505593US

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CIRCUITS TO SECURE THE ACCESS TO
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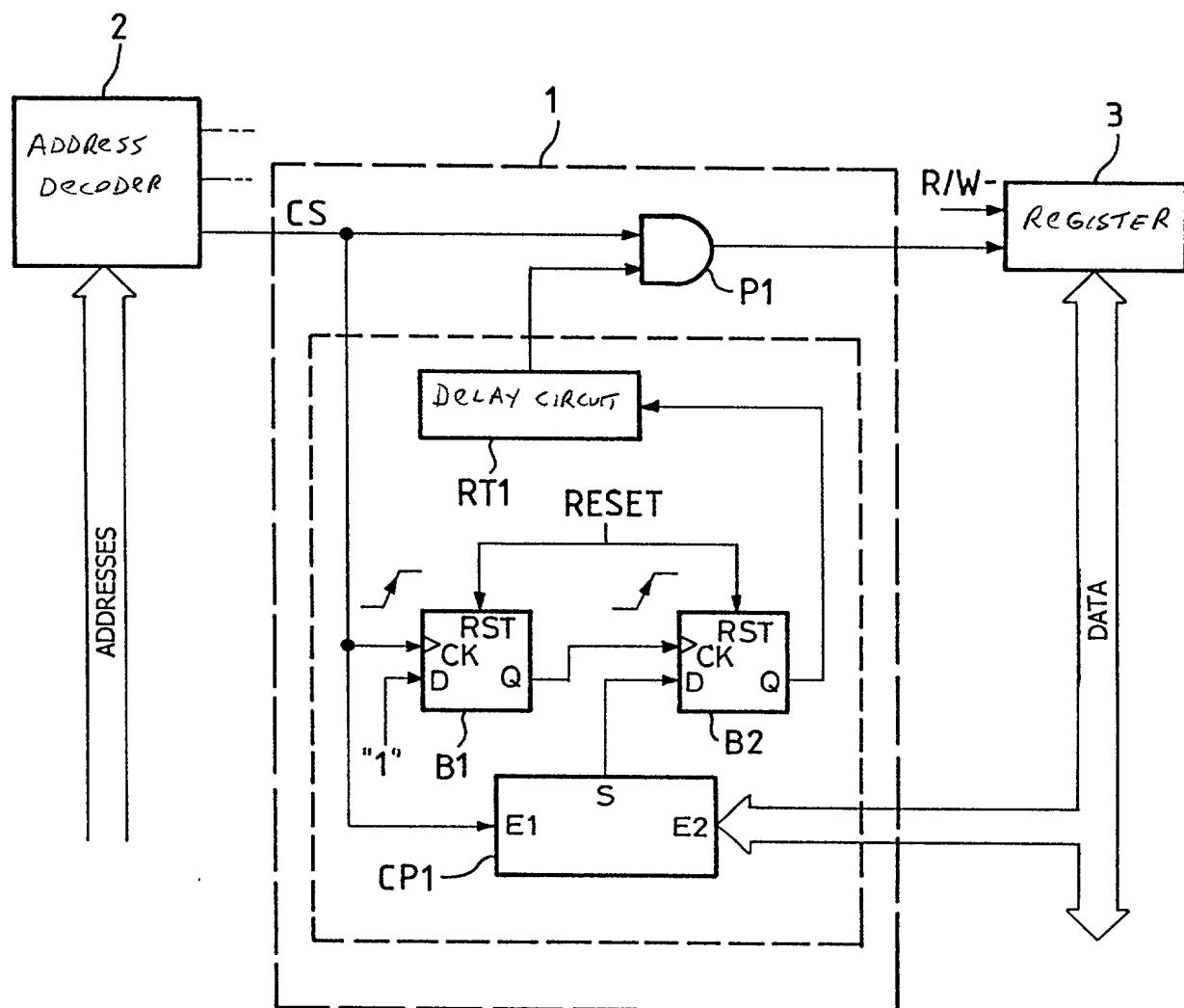
SUBMISSION OF PROPOSED MODIFICATIONS TO DRAWINGS

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modifications as indicated in red ink to label the blocks in
FIGS. 1-4.

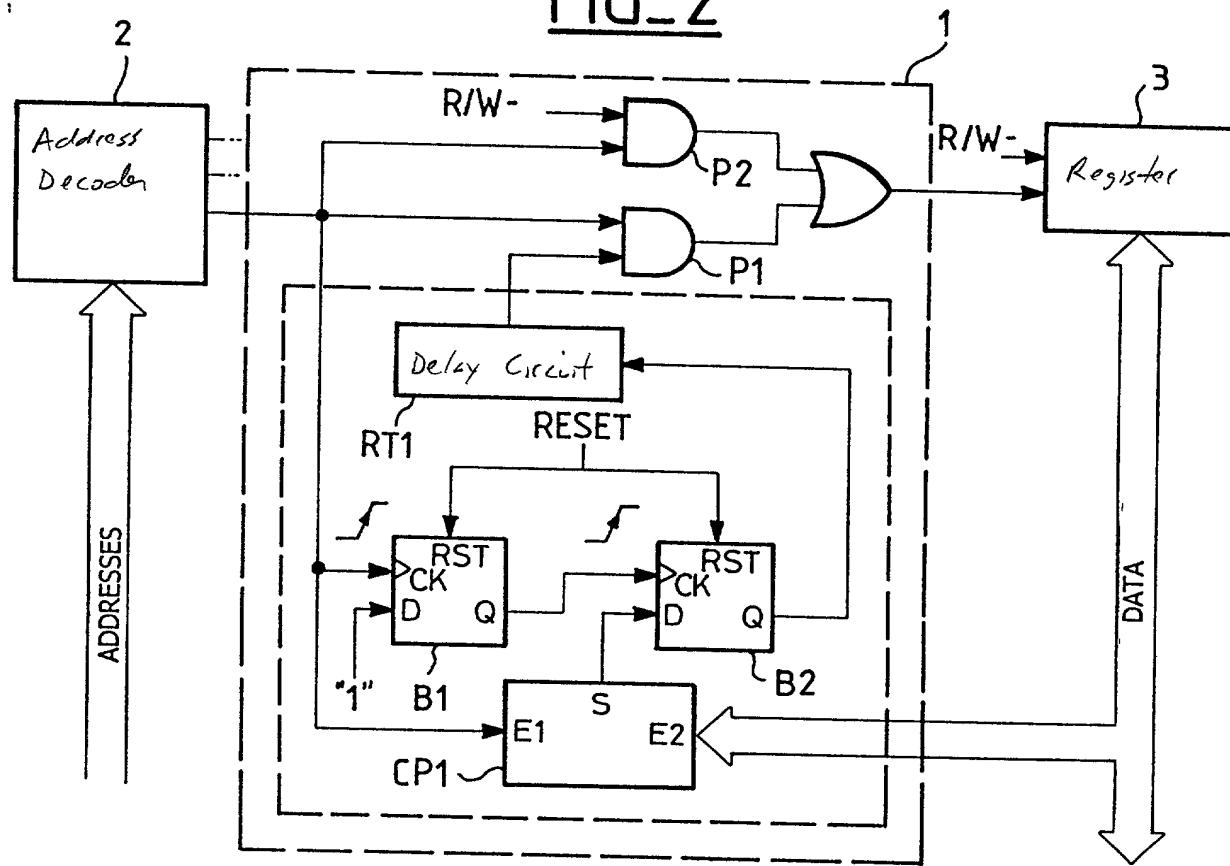
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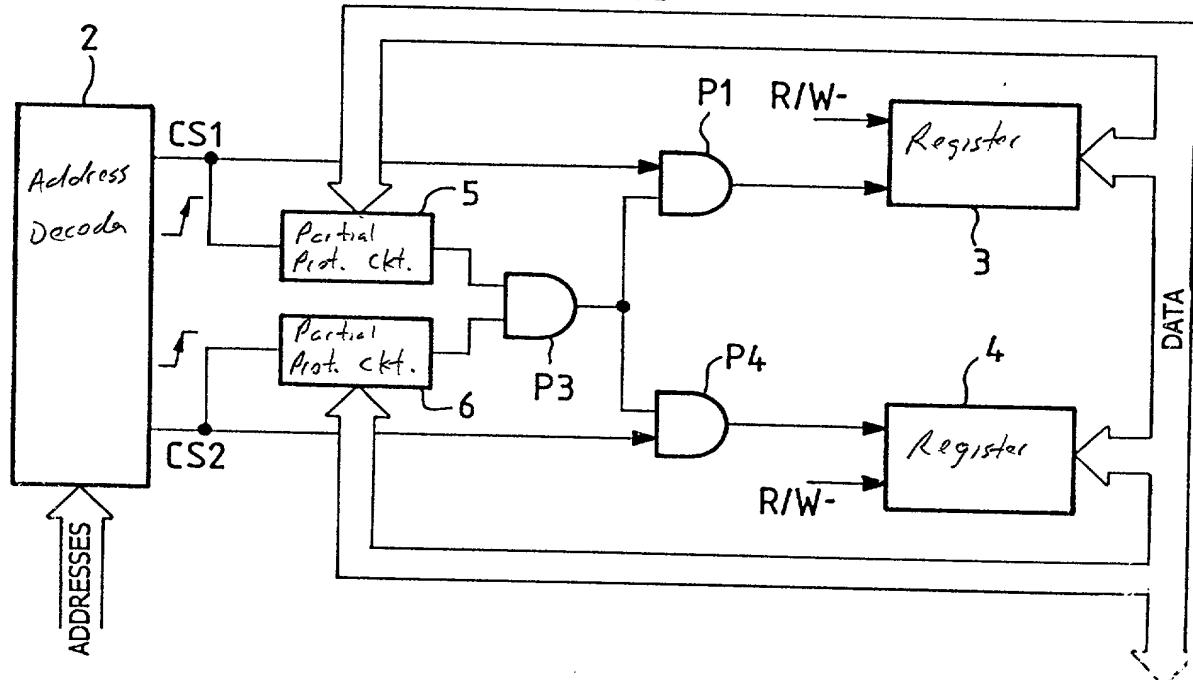
FIG_1

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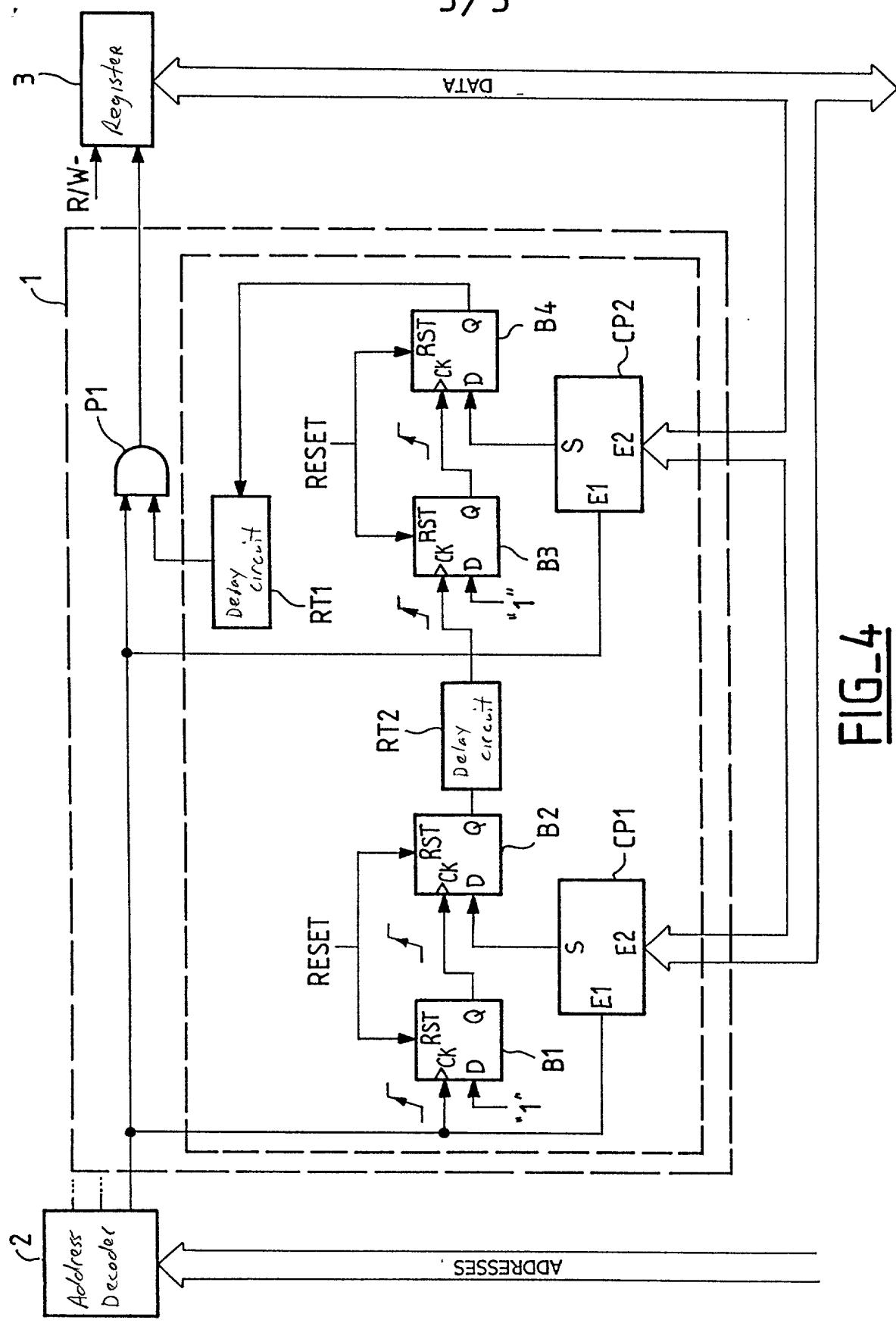
FIG_2



FIG_3



3/3



FIG_4

MICROPROCESSOR WITH PROTECTION CIRCUITS
TO SECURE THE ACCESS TO ITS REGISTERS

Field of the Invention

The present invention relates to microprocessors, and, more particularly, to a microprocessor provided with protection circuits designed to secure access to the registers of the 5 microprocessor.

Background of the Invention

A register in a microprocessor is generally selected as follows. The control unit of the 10 microprocessor generates the address of the register to be selected and applies it to the address bus of the microprocessor. This address is transmitted to an address decoder which then selects the register relating to the address by activating the selection 15 input of this register. The register can then be read or its contents can be modified. This register is, for example, an address register or an instruction register.

It sometimes happens that the contents of the 20 registers of the microprocessor are accidentally modified when a mistake is made, or when there is a malfunction of the system in the microprocessor, especially during the initialization of the microprocessor.

Summary of the Invention

An object of the invention is to provide a microprocessor that ensures secured access to its registers.

- 5 According to the invention, it is planned, after each initialization of the microprocessor, to prevent any access to the registers of this microprocessor and to permit access to a register only if a password proper to this register has been
10 presented at the data bus of the microprocessor during the first operation of selection of this register.

The microprocessor comprises an address bus, a data bus, a plurality of read accessible and write accessible registers, and an address decoder to select
15 the registers as a function of the address present in the address bus.

The microprocessor furthermore comprises a plurality of protection circuits each associated with a register of the microprocessor to secure the access to
20 the register. The protection circuits automatically block selection of the registers after each resetting of the microprocessor. The releasing of a protection circuit associated with a microprocessor register is done by the successive sending, on the data bus, of N
25 passwords proper to the register during N first operations for the selection of the register with $N \geq 1$. The selection of the register is effective only for the subsequent operations for the selection of the register up to the following resetting of the microprocessor.

30 As needed, the protection circuit may block the selection of the associated register during operations of read access and write access to this register, or only during write access operations. During the N first operations for the selection of the
35 associated register, each protection circuit compares the N data elements present in the data bus with the N passwords proper to the associated register. Each

protection circuit gets released for the subsequent operations of selection of the register up to the next resetting of the microprocessor if the N data elements correspond to the N passwords.

- 5 In one embodiment, only one password ($N=1$) is planned per register. The protection circuit then comprises a comparator circuit for the comparison, during the first operation of selection of the associated register, of the data element present in the
10 data bus with the password proper to the register and for the delivery of an output signal representing the result of the comparison. First means hold the output signal in the protection circuit until the following resetting of the microprocessor. Second means permit
15 the selection of the register for the subsequent selection operations of the register if the output signal indicates that the data present in the data bus of the microprocessor during the first operation of selection of the register corresponds to the password
20 associated with the register.

Brief Description of the Drawings

Other features and advantages of the invention shall appear from the following detailed
25 description made with reference to the appended drawings, of which:

FIG. 1 shows a first embodiment of a protection circuit according to the present invention to secure read access and write access to a register;

30 FIG. 2 shows a second embodiment of a protection circuit according to the present invention to secure write access to a register;

FIG. 3 shows a variation of the present invention by combining two protection circuits jointly
35 securing access to two registers; and

FIG. 4 shows a third embodiment of a protection circuit according to the present invention to secure read and write access to a register.

5 Detailed Description of the Preferred Embodiments

The registers referred to hereinafter in the description comprise a selection input, a read/write input to which a read/write signal R/W- is applied and a data input/output connected to the data bus of the
10 microprocessor. To implement the invention, a microprocessor, a portion of which is shown in FIG. 1, is provided with a protection circuit 1 to secure access to a register 3.

This protection circuit is interposed between
15 the output of an address decoder 2 responsible for selecting the register 3 and the selection input of the register 3. The output of the decoder delivers a selection signal CS. According to the invention, one protection circuit per register is provided.

20 According to the invention, the protection circuit 1 is designed to automatically block the transmission of the selection signal CS after each resetting of the microprocessor. The protection circuit 1 is then released by the sending of a password
25 proper to the register 3 on the data bus of the microprocessor during the first operation to select the register 3. The sending of a password on the data bus and the operation of selecting the register 3 are implemented, for example, during a cycle for writing
30 the password in the register 3.

The first selection operation is used to release the protection circuit 1. The selection of the register 3 is effective only for the subsequent operations of selection of the register, up to the
35 following resetting of the microprocessor. In the embodiment shown in FIG. 1, the protection circuit 1 blocks the selection of the register 3 during the

operations of read and write access to the register 3 after each resetting. According to one embodiment shown in FIG. 2, the protection circuit blocks the selection of the register 3 only during operations of
5 write access to the register 3.

Referring to FIG. 1, the protection circuit essentially has a comparator circuit CP1 for the comparison, during the first operation for the selection of the register 3, of the data present on the
10 data bus of the microprocessor with the password proper to the register 3. The comparator circuit CP1 delivers an output signal representing the result of the signal. The protection circuit also holds the output signal in the protection circuit up to the following resetting of
15 the microprocessor. Finally, the protection circuit permits selection of the register for the subsequent operations for selecting the register if the output signal indicates that the data element present on the data bus of the register during the first operation for
20 the selection of the register corresponds to the password associated with the register 3.

The comparator circuit CP1 has a selection input E1 connected to the output of the address decoder. This selection input E1 is responsible for
25 selecting the register 3. The comparator CP1 comprises a data input E2 to receive the data present on the data bus and an output S delivering a value representing the result of the comparison between the data element on the data bus and the password associated with the
30 register 3.

At its output S, it delivers a logic 1 if the two data elements are equal. Otherwise, it delivers a logic 0. The structure of a circuit of this kind is well known to those skilled in the art. The password
35 associated with the register 3 may be either stored permanently in the comparator circuit CP1 or given by an external peripheral device (not shown).

The result of a logic 1 or 0 of this comparison is held in the protection circuit 1 up to the following resetting of the microprocessor by two D type flip-flop circuits, B1 and B2, each having a clock 5 input CK, a signal input D, a resetting input RST and a signal output Q.

The clock input CK and the signal input D of the flip-flop circuit B1 respectively receive the selection signal CS and a logic 1. The signal input D 10 is, for example, connected to a power supply source of the microprocessor. The signal output Q of this flip-flop circuit is connected to the clock input CK of the flip-flop circuit B2. The signal input D of the flip-flop circuit B2 is connected to the output S of the 15 comparator circuit CP1. A resetting signal RESET is applied to the inputs RST of the flip-flop circuits B1 and B2 at each resetting of the microprocessor.

During the first operation for the selection of the register 3, the selection of the register 3 is 20 effective only to prevent the password present on the data bus during this operation from being written in the register 3. Hence, in order that the selection of the register 3 may be permitted only from the second selection operation of the register 3 onwards, the Q 25 output of the flip-flop circuit B2 is connected through a delay circuit RT1 to a first input of a two-input AND logic gate P1. The second input of the gate P1 is connected to the output of the address decoder 2, which is responsible for selecting the register 3. The 30 output of the gate P1 is connected to the selection input of the register 3. The delay circuit RT1 is preferably a shift register synchronized with the selection signal CS.

The protection circuit works as follows. At 35 each resetting of the microprocessor, the flip-flop circuits B1 and B2 are reset. During the first operation for the selection of the register 3, the

protection circuit 1 compares the data element present at the data output of the microprocessor with the password associated with the register 3. During this operation, the Q output of the flip-flop circuit B1

5 goes to a logic 1 and, on the resultant leading edge of the signal coming from this output, the Q output of the flip-flop circuit B2 delivers the result of the comparison. This result is then applied to the first input of the gate P1 with a delay to prevent the data

10 element present on the data bus from being written in the register 3 during this first operation.

If the delay circuit RT1 is a shift register synchronized with the signal CS, the result of the comparison is applied to the first input of the gate P1

15 only starting with the second operation for the selection of the register 3. The password associated with the register 3 is preferably a data element not usually planned in the program of the microprocessor. This prevents the protection circuit from being

20 accidentally released.

In a second embodiment shown in FIG. 2, the protection circuit is designed to secure only the write access of the register 3. The read access of the register 3 is never blocked. The releasing of the

25 protection circuit, however, must be done during the first operation for the selection of the register as in the protection circuit of FIG. 1.

Referring to FIG. 2, the protection circuit 1 is complemented by a second two-input AND logic gate P2

30 and one two-input OR logic gate. The gate P2 has a first input connected to the output of the decoder 2 responsible for selecting the register 3 and a second input to which the read/write signal R/W- is applied. The outputs of the gates P1 and P2 are each connected

35 to an input of the OR gate, and the output of the OR gate is connected to the selection input of the

register 3. Thus, the register 3 can be read at any time even if the protection circuit 1 is off.

In the case of an 8-bit microprocessor, there is a probability of $1/256$ ($256 = 2^8$) that the data present on the data bus during the first register 3 selection operation caused by a malfunctioning of the system will be the password associated with the register 3. To reduce this probability, it is proposed, as a variation, to combine the protection circuits of several registers with each other. This embodiment is shown in FIG. 3.

In the example of FIG. 3, the protection circuits of two registers are combined to secure their access. In this example, the address decoder is responsible for selecting registers of the microprocessor, especially two registers 3 and 4. The elements B1, B2, CP1 and RT1 of the protection circuit 1 of FIG. 1 are combined in a block 5. A two-input AND logic gate P3 is interposed between the output of the block 5 and the first input of the gate P1. The output of the block 5 corresponds to the output of the delay circuit RT1. The output of the decoder 2 responsible for selecting the register 3 is connected to the input of the block 5 and to the second input of the gate P1.

A block 6, identical to the block 5, and an AND logic gate P4 form the protection circuit of the register 4 as described in FIG. 1. The comparator circuit of the block 6 is responsible for comparing the data element present on the data bus with a password associated with the register 4, distinct from the one associated with the register 3. The output of the block 6 is connected to a second input of the gate P3. The output of the decoder 2 responsible for selecting the register 4 is connected to the input of the block 6 and to the second input of the gate P4.

To obtain access to the registers 3 and 4, the operation for the releasing of the protection

circuit of FIG. 3 includes obtaining a write access to each register by applying the corresponding password to the data bus. These two write access operations must be performed during the first selection of the register 5 3 and during the first selection of the register 4. The register 3 can be selected before or after the register 4.

To further reduce this probability, a third embodiment of the protection circuit 1 is illustrated 10 in FIG. 4. Access to the register 3 is secured by two passwords. These two passwords have to be placed on the data bus in a given order. For implementation of this protection circuit, the protection circuit of FIG. 1 is supplemented by two additional cascade-connected D 15 type flip-flop circuits, B3 and B4, a second comparator circuit CP2 and a second delay circuit RT2. The clock input CK of the flip-flop circuit B3 is connected to the Q output of the flip-flop circuit B2 by a second delay circuit RT2. A logic 1 is applied to the D input 20 of the flip-flop circuit B2, and its Q output is connected to the clock input CK of the flip-flop circuit B4.

The data input E2 of the comparator circuit CP2 is connected to the data bus, and its selection 25 input E1 is connected to the output of the address decoder responsible for selecting the register 3. The S output of the comparator CP2 is connected to the D input of the flip-flop circuit B4, and the Q output of the flip-flop circuit B4 is connected to the delay 30 circuit RT1. The two delay circuits are synchronized on the selection signal CS. The comparators CP1 and CP2 have the task, respectively, during the first and second operations for selecting the register 3, of comparing the data element present on the data bus with 35 the first password and second password of the register 3.

To release this protection circuit, it is necessary not only to give the two passwords associated with the register 3 on the data bus, but to give them in the right order. The security of the access to the 5 registers of the microprocessor is thereby improved. It is possible to further improve the security of the system by increasing the number of passwords associated with each register.

THAT WHICH IS CLAIMED IS:

1. A microprocessor comprising an address bus, a data bus, a plurality of read accessible and write accessible registers and an address decoder to select said registers as a function of the address
5 present in said address bus, wherein the microprocessor furthermore comprises a plurality of protection circuits each associated with a register of the microprocessor to secure the access to said register, said protection circuits automatically blocking the
10 selection of said registers after each resetting of the microprocessor, and wherein the releasing of a protection circuit associated with a microprocessor register is done by the successive sending, on the data bus, of N passwords proper to said register during N
15 first operations for the selection of said register with $N \geq 1$, the selection of said register being effective only for the subsequent operations for the selection of said register up to the next resetting of the microprocessor.

2. A microprocessor according to claim 1, wherein said protection circuit, after each resetting of the microprocessor, is arranged to block the selection of a register during operations of read
5 access and write access to said register.

3. A microprocessor according to claim 1 wherein said protection circuit, after each resetting of the microprocessor, is arranged to block the selection of a register only during operations of write
5 access to said register.

4. A microprocessor according to one of the claims 1 to 3, wherein each protection circuit is connected between an output of the address decoder

given the task of selecting the register associated
5 with said protection circuit and an input for the
selection of said associated register.

5. A microprocessor according to one of the
claims 1 to 4, wherein each protection circuit, during
the N first operations for the selection of the
associated register, is arranged to compare the N data
elements present on the data bus with the N passwords
proper to said associated register and gets released
for the subsequent operations of selection of said
register up to the next resetting of the microprocessor
if the N data elements correspond to the N passwords.

6. A microprocessor according to claim 4,
wherein one password is provided for each register, and
each protection circuit comprises:

- a comparator circuit for the comparison,
5 during the first operation of selection of the
associated register, of the data element present on the
data bus with the password proper to said register and
for the delivery of an output signal representing the
result of the comparison,
- 10 - first means for the holding, in the
protection circuit, of said output signal up to the
following resetting of the microprocessor,
 - second means to permit the selection of the
register for the subsequent selection operations of
15 said register if said output signal indicates that the
data present in the data bus of the microprocessor
during the first operation of selection of the register
corresponds to the password associated with said
register.

7. A microprocessor according to claim 6,
wherein the first means comprise first and second D
type flip-flop circuits, each having a clock input, a

signal input, a resetting input to which a signal for
5 resetting the microprocessor is applied, and a signal
output,

the first flip-flop circuit having its clock
input connected to the output of the address decoder
responsible for selecting the register associated with
10 said protection circuit and its signal input that
receives a signal corresponding to a logic « 1 »

and the second flip-flop circuit having its
clock input connected to the signal output of the first
flip-flop circuit, its signal input which receives the
15 output signal of the comparator circuit and its output
signal which thus delivers the output signal of the
comparator circuit up to the next resetting of the
microprocessor.

8. A microprocessor according to claim 7,
wherein the second means comprises an AND type two-
input logic gate having its first input is connected to
the output of the address decoder which has the task of
5 selecting the register associated with said protection
circuit, its second input is connected through a delay
circuit to the output signal of the second flip-flop
circuit of the first means, and its output connected to
the selection input of the associated register.

9. A microprocessor according to claim 8,
wherein said delay circuit is a shift register
synchronized with the operations for the selection of
said register.

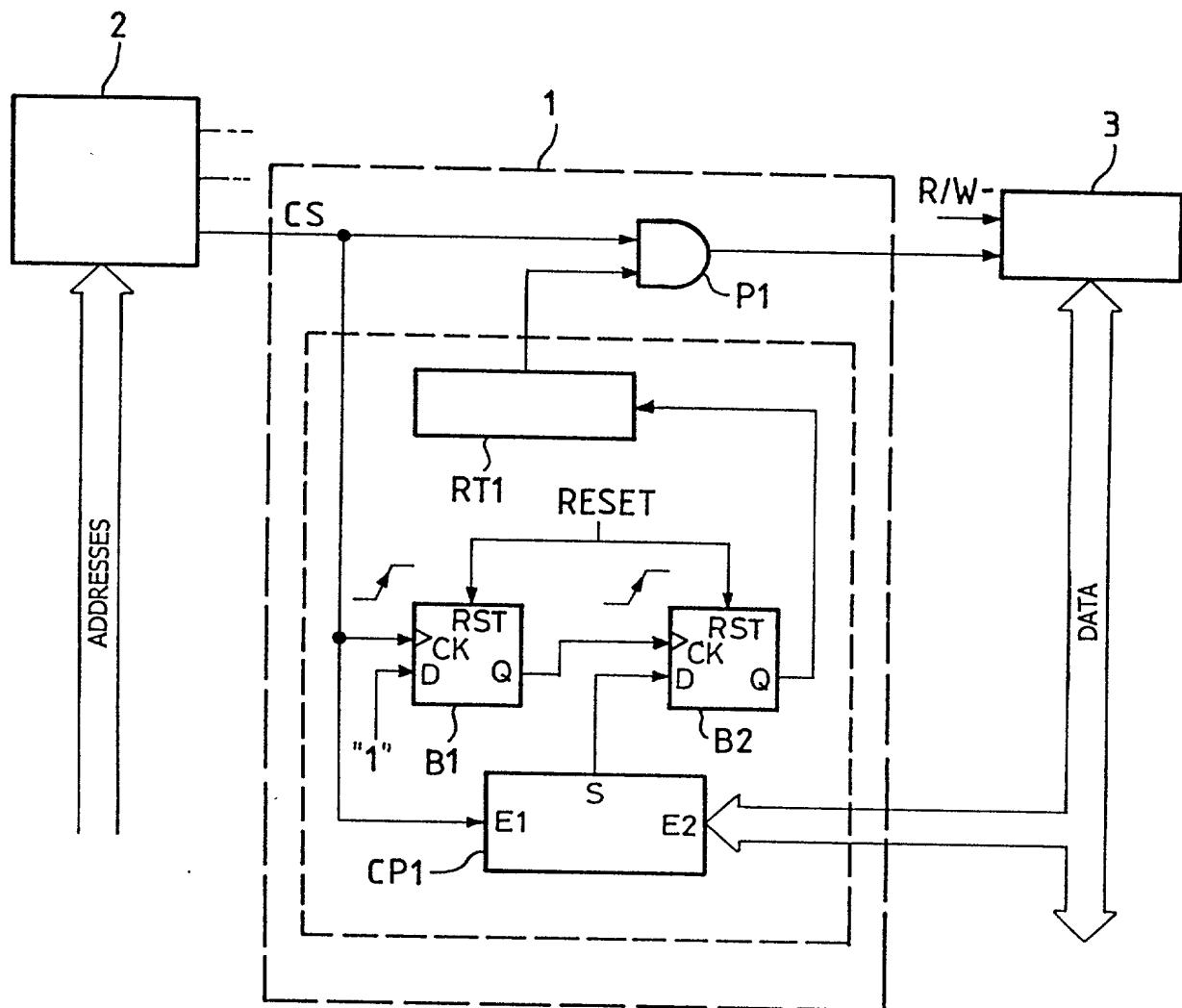
MICROPROCESSOR WITH PROTECTION CIRCUITS
TO SECURE THE ACCESS TO ITS REGISTERS

Abstract of the Disclosure

A microprocessor is provided with protection circuits to secure access to its registers. The microprocessor includes a plurality of protection circuits, each associated with a register of the

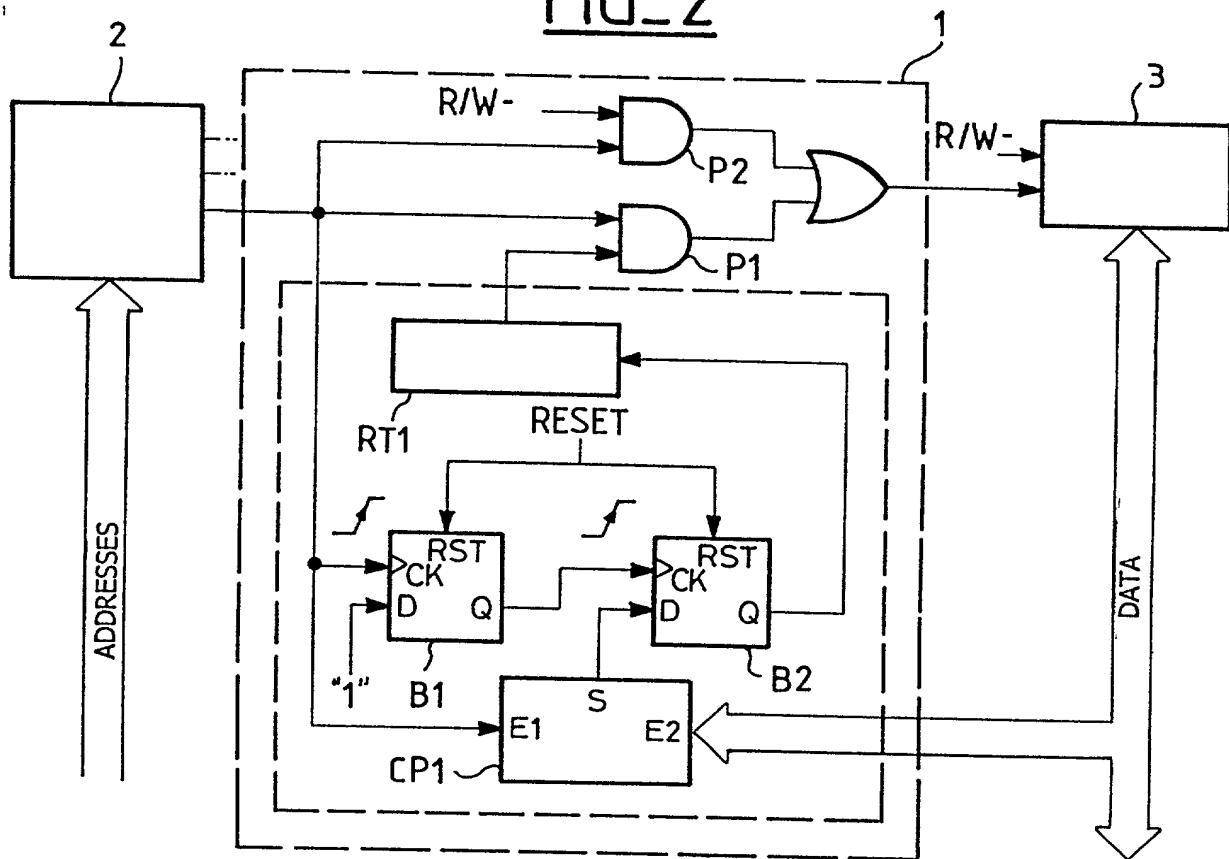
5 microprocessor. The protection circuits automatically block selection of the registers after each resetting of the microprocessor. The releasing of a protection circuit associated with a register is done by the successive sending, on the data bus, of N passwords

10 proper to the register during N first operations for the selection of the register with $N \geq 1$. The selection of the register is effective only for the subsequent operations for selection of the register up to the next resetting of the microprocessor.

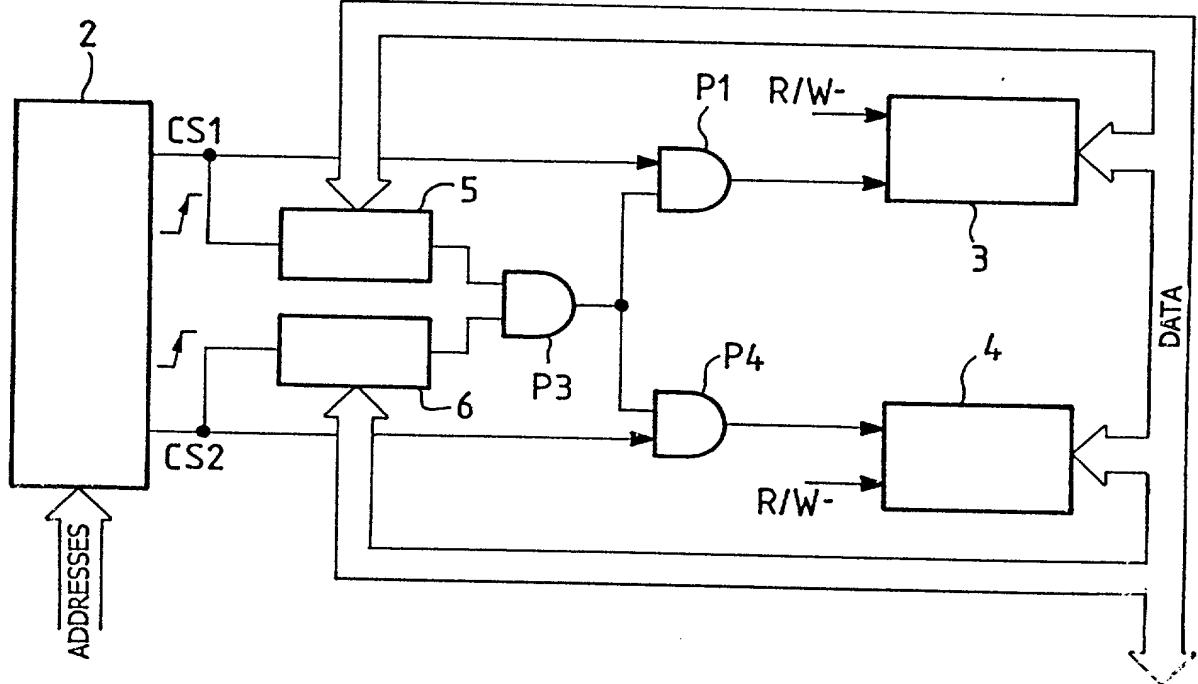
FIG_1

2 / 3

FIG_2



FIG_3



FIG_4

